MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 2, 2015/2016

TAO1221 – COMPUTER ARCHITECTURE AND ORGANIZATION

(All sections / Groups)

02 MARCH 2016
2.30 p.m. – 4.30 p.m.
(2 hours)

INSTRUCTIONS TO STUDENTS

1. This Question paper consists of 5 pages including cover page with 6 Questions only.

2. Attempt **FIVE** out of **SIX** questions. All questions carry equal marks and the distribution of the marks for each question is given.

3. Please print all your answers in the Answer Booklet provided.

QUESTION 1

(a) Contemporary computer designs are based on concepts developed by John von Neumann at the Institute for Advanced Studies, Princeton. Describe the **THREE (3)** key concepts of von Neumann architecture. [3 marks]

(b) Consider a hypothetical 24-bit microprocessor having 24-bit instructions composed of two fields: the first byte contains the opcode and the remainder contains the immediate operand or operand address. Assume that the word size is 24 bits.

i. What is the maximum directly addressable memory capacity (in bytes)?

ii. Discuss the impact on the system speed if the microprocessor bus has a 16-bit local address bus and an 8-bit local data bus.

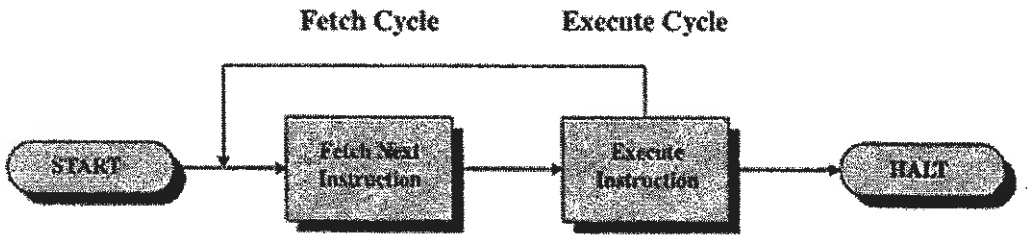
iii. How many bits are needed for the program counter and the instruction register, if the instruction register is to contain the whole instruction or only the opcode? [1 + 3 + 3 marks]

QUESTION 2

(a) List **THREE (3)** major components in computer architecture. Explain the function of each component. [6 marks]

(b) Explain **TWO (2)** basic tasks performed by a control unit. [2 marks]

(c) In instruction processing, the basic instruction cycle is shown below:



Assume that the processor contains a program counter (PC), a memory address register (MAR), a memory buffer register (MBR), and an instruction register (IR). List the steps of actions taking place during the **Fetch Cycle**.

[2 marks]

Continued ....

QUESTION 3

(a) Given that A = $(23)_{10}$, B = $(41)_{10}$, and C = $(-36)_{10}$.

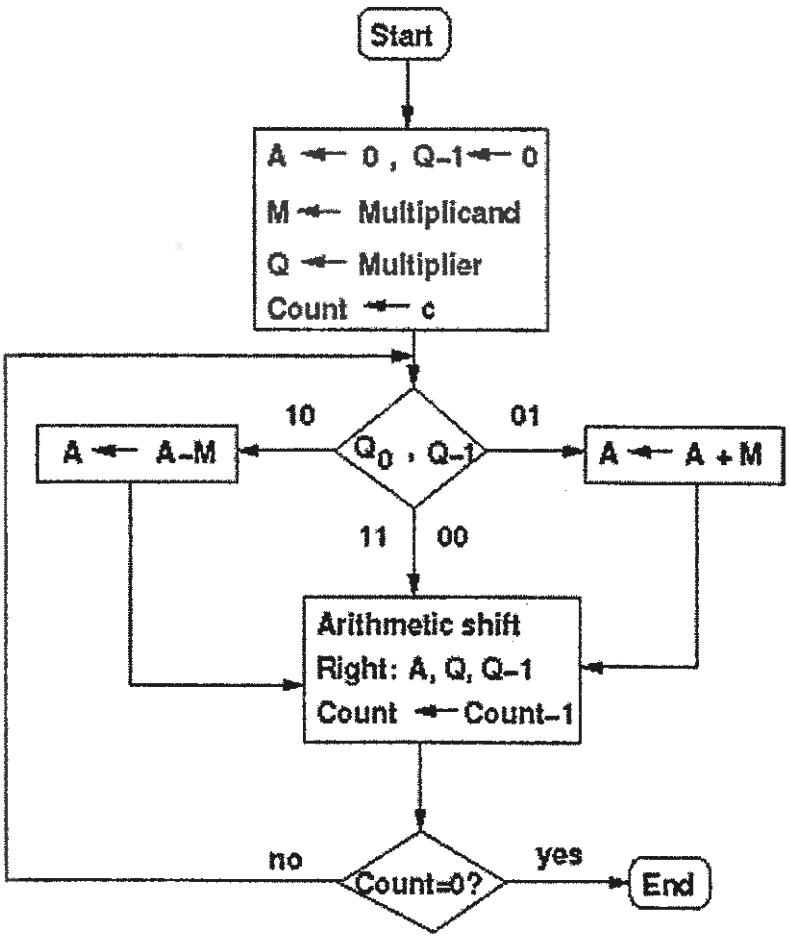
i. Represent A, B, and C in **8-bit two's complement** form. [3 marks]

ii. Perform the following arithmetic operations in two's complement representation. Detect and provide reason if any overflow occurs.

a. [A + B] [1 mark]

b. [C – B] [1 mark]

(b) Given the Booth's Algorithm flowchart:



Show the steps using Booth's Algorithm for performing the multiplication of two **4-bit two's complement** binary numbers as given below:

Multiplicand (M) = $(0011)_2$ or $(3)_{10}$
Multiplier (Q) = $(1011)_2$ or $(-5)_{10}$

[5 marks]

Continued ....

QUESTION 4

(a) List any **SIX (6)** of the most common addressing techniques used in microprocessors. [3 marks]

(b) Given the following registers and memory values for an Intel 8085 microprocessor:

Registers

A 85H

B 00H C 00H

D 77H E 10H

H 08H L 45H

Memory

Location	Contents
0844H	43H
0845H	44H
7710H	B6H
7756H	7CH

What is the value in the Accumulator (Register A) when the following instructions are executed in sequence? Show the result for each instruction execution.

i. MVI B, 56H
ii. LDAX D
iii. MOV M,A
iv. MVI A,ACH
v. MOV D,A
vi. MOV A,M
vii. ADD M
viii. ADD E

[4 marks]

(c) Certain instructions in assembly language change the sequence of instruction execution. When this type of instructions is executed, the operation performed by the processor is to update the Program Counter (PC) to contain the address of the next instruction in memory. These operations are called transfer-of-control; examples include Branch, Skip, and Procedure Call. Briefly discuss **THREE (3)** reasons why these operations are required. [3 marks]

Continued ....

QUESTION 5

(a) In caches, associative mapping is one of the mapping techniques used in microprocessor. What is the advantage and disadvantage of this technique?

[2 marks]

(b) Consider a machine with a byte addressable main memory of 28 bytes and block size of 4 bytes. Assume that a direct mapped cache consisting of 8 lines is used with this machine. How is an 8-bit memory address divided into tag, line number, and byte number? Show the address format.

[5 marks]

(c) Compare the following semiconductor memory types in terms of **category**, **erasure**, **write mechanism**, and **volatility**:

i. Random-access memory (RAM)
ii. Programmable read-only memory (PROM)
iii. Flash memory

[3 marks]

QUESTION 6

(a) An I/O module is used to link external devices to the computer. Briefly discuss **FIVE (5)** categories of functions for an I/O module. [5 marks]

(b) A bus organization is one of the approaches that could be used in the implementation of symmetric multiprocessor organization. Discuss **THREE (3)** attractive features of this approach. [3 marks]

(c) Snoopy protocols distribute the responsibility for maintaining cache coherence among all of the cache controllers in a multiprocessor system. One of the basic approaches in snoopy protocols is 'write invalidate'. Briefly explain how 'write invalidate' is able to maintain coherence among processors. [2 marks]

End of Paper.